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Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of Semiconductor Devices [1]

This standard is issued under the fixed designation F1192; the number immediately following the designation indicates the year of original adoption or, in the case of revision, the year of last revision. A number in parentheses indicates the year of last reapproval. A superscript epsilon (ε) indicates an editorial change since the last revision or reapproval.

This standard has been approved for use by agencies of the U.S. Department of Defense.

1. Scope

1.1 This guide defines the requirements and procedures for testing integrated circuits and other devices for the effects of single event phenomena (SEP) induced by irradiation with heavy ions having an atomic number $Z \geq 2$. This description specifically excludes the effects of neutrons, protons, and other lighter particles that may induce SEP via another mechanism. SEP includes any manifestation of upset induced by a single ion strike, including soft errors (one or more simultaneous reversible bit flips), hard errors (irreversible bit flips), latchup (persistent high conducting state), transients induced in combinatorial devices which may introduce a soft error in nearby circuits, power field effect transistor (FET) burn-out and gate rupture. This test may be considered to be destructive because it often involves the removal of device lids prior to irradiation. Bit flips are usually associated with digital devices and latchup is usually confined to bulk complementary metal oxide semiconductor, (CMOS) devices, but heavy ion induced SEP is also observed in combinatorial logic programmable read only memory, (PROMs), and certain linear devices that may respond to a heavy ion induced charge transient. Power transistors may be tested by the procedure called out in Method 1080 of MIL STD 750.

1.2 The procedures described here can be used to simulate and predict SEP arising from the natural space environment, including galactic cosmic rays, planetary trapped ions, and solar flares. The techniques do not, however, simulate heavy ion beam effects proposed for military programs. The end product of the test is a plot of the SEP cross section (the number of upsets per unit fluence) as a function of ion LET (linear energy transfer or ionization deposited along the ion's path through the semiconductor). This data can be combined with the system's heavy ion environment to estimate a system upset rate.

1.3 Although protons can cause SEP, they are not included in this guide. A separate guide addressing proton induced SEP is being considered.

1.4 The values stated in SI units are to be regarded as standard. No other units of measurement are included in this standard.

1.5 *This standard does not purport to address all of the safety concerns, if any, associated with its use. It is the responsibility of the user of this standard to establish appropriate safety, health, and environmental practices and determine the applicability of regulatory limitations prior to use.*

1.6 *This international standard was developed in accordance with internationally recognized principles on standardization established in the Decision on Principles for the Development of International Standards, Guides and Recommendations issued by the World Trade Organization Technical Barriers to Trade (TBT) Committee.*

2. Referenced Documents

2.1 *Military Standard:*[2]
750 Method 1080

3. Terminology

3.1 *Definitions of Terms Specific to This Standard:*

3.1.1 *DUT*—device under test.

3.1.2 *fluence*—the flux integrated over time, expressed as ions/cm^2.

3.1.3 *flux*—the number of ions/s passing through a one cm^2 area perpendicular to the beam (ions/cm ^{2}-s).

3.1.4 *LET*—the linear energy transfer, also known as the stopping power dE/dx, is the amount of energy deposited per unit length along the path of the incident ion, typically normalized by the target density and expressed as MeV-cm^2/mg.

3.1.4.1 *Discussion*—LET values are obtained by dividing the energy per unit track length by the density of the irradiated medium. Since the energy lost along the track generates

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[2] Available from Standardization Documents Order Desk, Bldg. 4, Section D, 700 Robbins Ave., Philadelphia, PA 19111–5094.

electron-hole pairs, one can also express LET as charge deposited per unit path length (for example, picocoulombs/micron) if it is known how much energy is required to generate an electron-hole pair in the irradiated material. (For silicon, 3.62 eV is required per electron-hole pair.)

A correction, important for lower energy ions in particular, is made to allow for the loss of ion energy after it has penetrated overlayers above the device sensitive volume. Thus the ion's energy, E, at the sensitive volume is related to its initial energy, E_O, as:

$$E_s = E_o - \int_o^{(t/\cos\theta)} \left(\frac{dE(x)}{dx} \right) dx$$

where t is the thickness of the overlayer and θ is the angle of the incident beam with respect to the surface normal. The appropriate LET would thus correspond to the modified energy, E.

A very important concept, but one which is by no means universally true, is the *effective LET*. The effective LET applies for those soft error mechanisms where the device susceptibility depends, in reality, on the charge deposited within a sensitive volume that is thin like a wafer. By equating the charge deposited at normal incidence to that deposited by an ion with incident angle θ, we obtain:

$$\text{LET(effective)} = \text{LET(normal)}/\cos\theta \quad \theta < 60°$$

Because of this relationship, one can sometimes test with a single ion at two different angles to correspond to two different (effective) LETs. Note that the effective LET at high angles may not be a realistic measure (see also 6.6). Note also that the above relationship breaks down when the lateral dimensions of the sensitive volume are comparable to its depth, as is the case with VLSI and other modern high density ICs.

3.1.5 *single event burnout*—SEB (also known as SEBO) may occur as a result of a single ion strike. Here a power transistor sustains a high drain-source current condition, which usually culminates in device destruction.

3.1.6 *single event effects*—SEE is a term used earlier to describe many of the effects now included in the term SEP.

3.1.7 *single event gate rupture*—SEGR (also known as SEGD) may occur as a result of a single ion strike. Here a power transistor sustains a high gate current as a result of damage of the gate oxide.

3.1.8 *single event functionality interrupt*—SEFI may occur as a result of a single ion striking a special device node, used for an electrical functionality test.

3.1.9 *single event hard fault*—often called hard error, is a permanent, unalterable change of state that is typically associated with permanent damage to one or more of the materials comprising the affected device.

3.1.10 *single event latchup*—SEL is an abnormal low impedance, high-current density state induced in an integrated circuit that embodies a parasitic pnpn structure operating as a silicon controlled rectifier.

3.1.11 *single event phenomena*—SEP is the broad category of all semiconductor device responses to a single hit from an energetic particle. This term would also include effects induced by neutrons and protons, as well as the response of power transistors—categories not included in this guide.

3.1.12 *single event transients, (SET)*—SET's are SE-caused electrical transients that are propagated to the outputs of combinational logic IC's. Depending upon system application of these combinational logic IC's, SET's can cause system SEU.

3.1.13 *single event upset, (SEU)*—comprise soft upsets and hard faults.

3.1.14 *soft upset*—the change of state of a single latched logic state from one to zero, or vice versa. The upset is "soft" if the latch can be rewritten and behave normally thereafter.

3.1.15 *threshold LET*—for a given device, the threshold LET is defined as the minimum LET that a particle must have to cause a SEU at θ = 0 for a specified fluence (for example, 10^6 ions/cm^2). In some of the literature, the threshold LET is also sometimes defined as that LET value where the cross section is some fraction of the "limiting" cross section, but this definition is not endorsed herein.

3.1.16 *SEP cross section*—is a derived quantity equal to the number of SEP events per unit fluence.

3.1.16.1 *Discussion*—For those situations that meet the criteria described for usage of an effective LET (see 3.1.4), the SEP cross section can be extended to include beams impinging at an oblique angle as follows:

$$\sigma = \frac{\text{number of upsets}}{\text{fluence} \times \cos\theta}$$

where θ = angle of the beam with respect to the perpendicularity to the chip. The cross section may have units such as cm^2/device or cm^2/bit or μm^2/bit. In the limit of high LET (which depends on the particular device), the SEP cross section will have an area equal to the sensitive area of the device (with the boundaries extended to allow for possible diffusion of charge from an adjacent ion strike). If any ion causes multiple upsets per strike, the SEP cross section will be proportionally higher. If the thin region waferlike assumption for the shape of the sensitive volume does not apply, then the SEP cross section data become a complicated function of incident ion angle. As a general rule, high angle tests are to be avoided when a normal incident ion of the same LET is available.

A limiting or asymptotic cross section is sometimes measured at high LET whenever all particles impinging on a sensitive area of the device cause upset. One can establish this value if two measurements, having a different high LET, exhibit the same cross sections.

3.2 *Abbreviations:*

3.2.1 *ALS*—advanced low power Schottky.

3.2.2 *CMOS*—complementary metal oxide semiconductor device.

3.2.3 *FET*—field effect transistor.

3.2.4 *IC*—integrated circuit.

3.2.5 *NMOS*—*n*-type-channel metal oxide semiconductor device.

3.2.6 *PMOS*—*p*-type-channel metal oxide semiconductor device.

3.2.7 *PROM*—programmable read only memory.

3.2.8 *RAM*—random access memory.

3.2.9 *VLSI*—very large scale integrated circuit.

4. Summary of Guide

4.1 The SEP test consists of irradiation of a device with a prescribed heavy ion beam of known energy and flux in such a way that the number of single event upsets or other phenomena can be detected as a function of the beam fluence (particles/cm^2). For the case where latchup is observed, a series of measurements is required in which the fluence is recorded at which latchup occurs, in order to obtain an average fluence.

4.2 The beam LET, equivalent to the ion's stopping power, *dE/dx*, (energy/distance), is a fundamental measurement variable. A full device characterization requires irradiation with beams of several different LETs that in turn requires changing the ion species, energy, or, in some cases, angle of incidence with respect to the chip surface.

4.3 The final useful end product is a plot of the upset rate or cross section as a function of the beam LET or, equivalently, a plot of the average fluence to cause upset as a function of beam LET. These comments presume that LET, independent of *Z*, is a determinant of SE vulnerability. In cases where charge density (or charge density and total charge) per unit distance determine device response to SEs, results provided solely in terms of LET may be incomplete or inaccurate, or both.

4.4 *Test Conditions and Restrictions*—Because many factors enter into the effects of radiation on the device, parties to the test should establish and record the test conditions to ensure test validity and to facilitate comparison with data obtained by other experimenters testing the same type of device. Important factors which must be considered are:

4.4.1 *Device Appraisal*—A review of existing device data to establish basic test procedures and limits (see 8.1),

4.4.2 *Radiation Source*—The type and characteristics of the heavy ion source to be used (see 7.1),

4.4.3 *Operating Conditions*—The description of the testing procedure, electrical biases, input vectors, temperature range, current-limiting conditions, clocking rates, reset conditions, etc., must be established (see Sections 6, 7, and 8),

4.4.4 *Experimental Set-Up*—The physical arrangement of the accelerator beam, dosimetry electronics, test device, vacuum chamber, cabling and any other mechanical or electrical elements of the test (see Section 7),

4.4.5 *Upset Detection*—The basis for establishing upset must be defined (for example, by comparison of the test device response with some reference states, or by comparison of post-irradiation bit patterns with the pre-irradiation pattern, and the like (see 7.4)). Tests of heavy ion induced transients require special techniques whose extent depends on the objectives and resources of the experimenter,

4.4.6 *Dosimetry*—The techniques to be used to measure ion beam fluxes and fluence.

4.4.7 *Flux Range*—The range of heavy ion fluxes (both average and instantaneous) must be established in order to provide proper dosimetry and ensure the absence of collective effects on device response. For heavy ion SEP tests a normal flux range will be 10^2 to 10^5 ions/cm^2-s. However, higher fluxes are acceptable if it can be established that dosimetry and tester limits, coincident upset effects, device heating, and the like, are properly accounted for. Such higher limits may be needed for testing future smaller geometry parts.

4.4.8 *Particle Fluence Levels*—The minimum fluence is that fluence required to establish that an observance of no upsets corresponds to an acceptable upper bound on the upset cross section with a given confidence. Sufficient fluence should be provided to also ensure that the measured number of upset events provides an upset cross section whose magnitude lies within acceptable error limits (see 8.2.7.2). In practice, a fluence of 10^7 ions/cm^2 will often meet these requirements.

4.4.9 *Accumulated Total Dose*—The total accumulated dose shall be recorded for each device. However, it should be noted that the average dose actually represents a few heavy ion tracks, <10 nm in diameter, in each charge collection region, so this dose may affect the device physics differently than a uniform (for example, gamma) dose deposition. In particular, it is sometimes observed that accumulated dose delivered by heavy ions is less damaging than that delivered with uniform dose deposition.

4.4.10 *Range of Ions*—The range or penetration depth of the energetic ions is an important consideration. An adequate range is especially crucial in detecting latchup, because the relevant junction is often buried deep below the active chip. Some test requirements specify an ion range of >30 μm. The U.C. Berkeley 88-inch cyclotron and the Brookhaven National Laboratory Van de Graaff have adequate energy for most ions, but not all. Gold data at BNL is frequently too limited in range to give consistent results when compared to nearby ions of the periodic table. Medium-energy sources, such as the K500 cyclotron at Texas A & M, easily satisfy all range requirements. High-energy machines that simulate cosmic ray energies, such as GANIL (Caen, France) and the cyclotron at Darmstadt, Germany, provide greater range.

5. Significance and Use

5.1 Many modern integrated circuits, power transistors, and other devices experience SEP when exposed to cosmic rays in interplanetary space, in satellite orbits or during a short passage through trapped radiation belts. It is essential to be able to predict the SEP rate for a specific environment in order to establish proper techniques to counter the effects of such upsets in proposed systems. As the technology moves toward higher density ICs, the problem is likely to become even more acute.

5.2 This guide is intended to assist experimenters in performing ground tests to yield data enabling SEP predictions to be made.

6. Interferences

6.1 There are several factors which need to be considered in accommodating interferences affecting the test. Each is described herein.

6.2 *Ion Beam Pile-up*—When an accelerator is being chosen to perform a SEP test, the machine duty cycle needs to be